ON Semiconductor®

P3P623S00B/E

Timing-Safe™ Peak EMI Reduction IC

General Features

- Clock distribution with Timing-Safe™ Peak EMI Reduction
- Input frequency range: 20MHz - 50MHz
- 2 different Spread Selection options
- Spread Spectrum can be turned ON/OFF
- External Input-Output Delay Control option
- Supply Voltage: 3.3V±0.3V
- P3P623S00B: 8 pin SOIC
  P3P623S00E:16 pin TSSOP
- The First True Drop-in Solution

Functional Description

P3P623S00B/E is a versatile, 3.3V Zero-delay buffer designed to distribute Timing-Safe™ clocks with Peak EMI reduction. P3P623S00B is an eight-pin version, accepts one reference input and drives out one low-skew Timing-Safe™ clock. P3P623S00E accepts one reference input and drives out eight low-skew Timing-Safe™ clocks.

P3P623S00B/E has an SS% that selects 2 different Deviation and associated Input-Output Skew (T_{SKEW}). Refer to the *Spread Spectrum Control* and *Input-Output Skew* table for details.

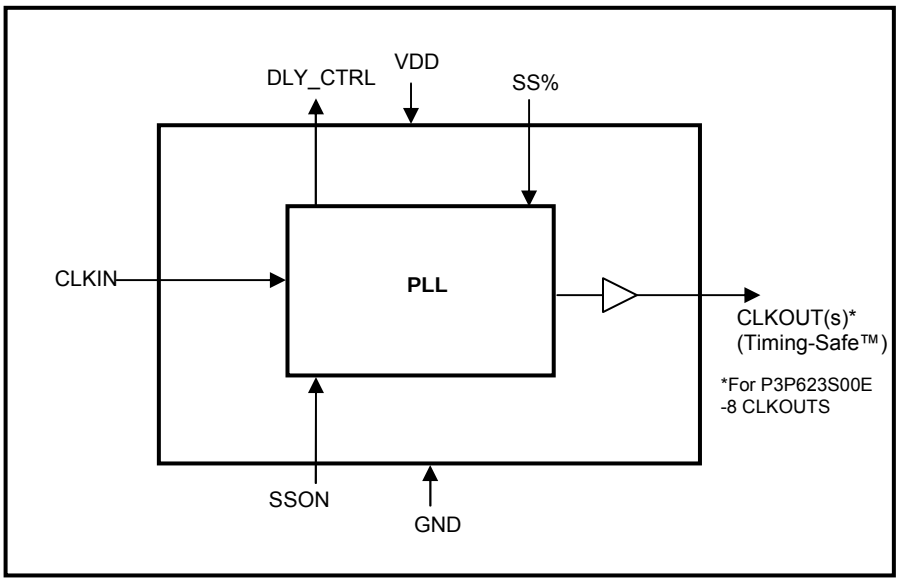
P3P623S00E has a CLKOUT for adjusting the Input-Output clock delay, depending upon the value of capacitor connected at this pin to GND.

P3P623S00B/E operates from a 3.3V supply and is available in two different packages, as shown in the ordering information table.

Application

P3P623S00B/E is targeted for use in Displays and memory interface systems.

General Block Diagram



Publication Order Number:
P3P623S00/D

Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer PCBs, etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The P3P623S00B/E uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation

Zero Delay and Skew Control

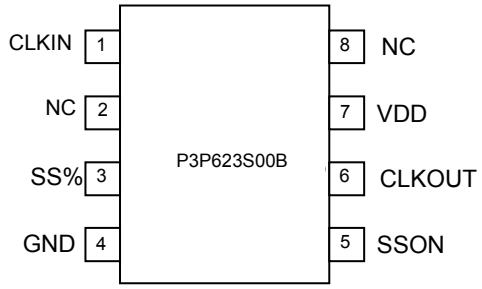
All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero input-output delay.

Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration for P3P623S00B

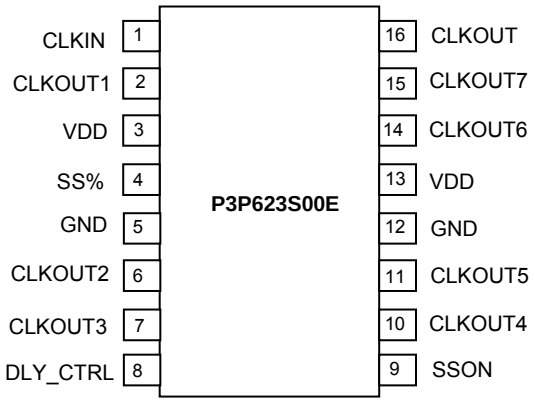


Pin Description for P3P623S00B

Pin #	Pin Name	Type	Description
1	CLKIN[1]	I	External reference Clock input , 5V tolerant input
2	NC		No Connect
3	SS%[3]	I	Spread Spectrum Selection. Has an internal pull up resistor
4	GND	P	Ground
5	SSON[3]	I	Spread Spectrum enable and disable option. When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. Has an internal pull up resistor
6	CLKOUT[2]	O	Buffered clock output[4]
7	VDD	P	3.3V supply
8	NC		No Connect

Notes: 1. Weak pull down
2. Weak pull-down on all outputs
3. Weak pull-up on these Inputs
4. Buffered clock output is Timing-Safe™

Pin Configuration



Pin Description for P3P623S00E

Pin #	Pin Name	Type	Description
1	CLKIN[1]	I	External reference Clock input, 5V tolerant input
2	CLKOUT1[2]	O	Buffered clock output[4]
3	V_{DD}	P	3.3V supply
4	SS%[3]	I	Spread Spectrum Selection. Refer to the *Spread Spectrum Control* and *Input-Output Skew* Table. Has an internal pull up resistor.
5	GND	P	Ground
6	CLKOUT2[2]	O	Buffered clock output[4]
7	CLKOUT3[2]	O	Buffered clock output[4]
8	DLY_CTRL	O	External Input-Output Delay control.
9	SSON[3]	I	Spread Spectrum enable and disable option. When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. Has an internal pull up resistor.
10	CLKOUT4[2]	O	Buffered clock output[4]
11	CLKOUT5[2]	O	Buffered clock output[4]
12	GND	P	Ground
13	V_{DD}	P	3.3V supply
14	CLKOUT6[2]	O	Buffered clock output[4]
15	CLKOUT7[2]	O	Buffered clock output[4]
16	CLKOUT[2]	O	Buffered clock output[4]

Notes: 1. Weak pull down
2. Weak pull-down on all outputs
3. Weak pull-up on these Inputs
4. Buffered clock output is Timing-Safe™

Spread Spectrum Control and Input-Output Skew Table

Device	Input Frequency	SS %	Deviation	Input-Output Skew ($\pm T_{SKEW}$)
P3P623S00B/E	32MHz	0	±0.25 %	0.125
		1	±0.50 %	0.25

Note: T_{SKEW} is measured in units of the Clock Period

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage to Ground Potential	-0.5 to +4.6	V
VIN	DC Input Voltage (CLKIN)	-0.5 to +7	
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+85	℃
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage[5]				0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = VDD			100	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8mA			0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = -8mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs			27	mA
Z_o	Output Impedance			23		Ω

Notes: 5. CLKIN input has a threshold voltage of VDD/2
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

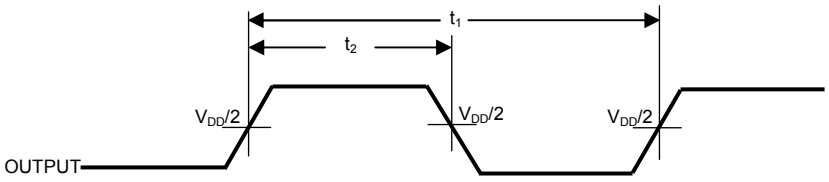
Switching Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Frequency		20		50	MHz
Output Frequency	30pF load	20		50	MHz
Duty Cycle [6,7] = (t_2 / t_1) * 100	Measured at VDD/2	40	50	60	%
Output Rise Time [7, 8]	Measured between 0.8V and 2.0V			2.5	nS
Output Fall Time [7, 8]	Measured between 2.0V and 0.8V			2.5	nS
Output-to-output skew [7, 8]	All outputs equally loaded with SSOFF			250	pS
Delay, CLKIN Rising Edge to CLKOUT Rising Edge [8]	Measured at VDD /2 with SSOFF			±350	pS
Device-to-Device Skew [8]	Measured at VDD/2 on the CLKOUT pins of the device			700	pS
Cycle-to-Cycle Jitter [7, 8]	Loaded outputs			±250	pS
PLL Lock Time [8]	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

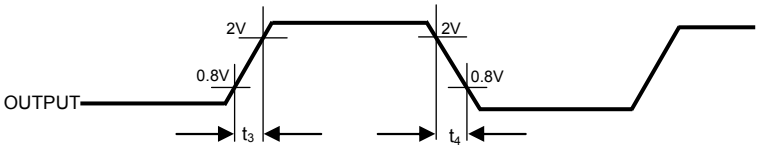
Note: 7. All parameters specified with 30pF loaded outputs.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

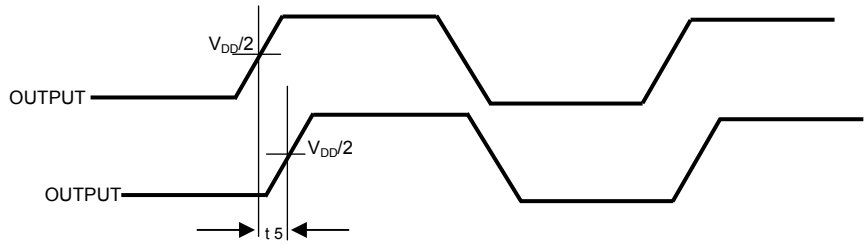
Duty Cycle Timing



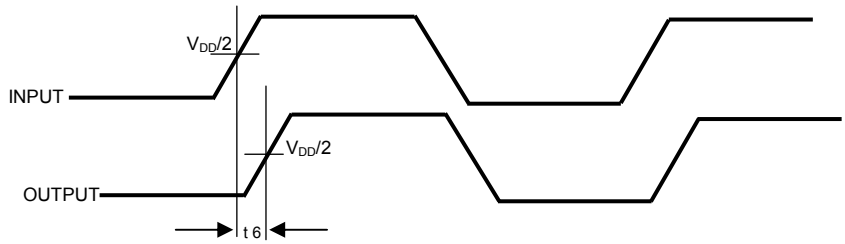
All Outputs Rise/Fall Time



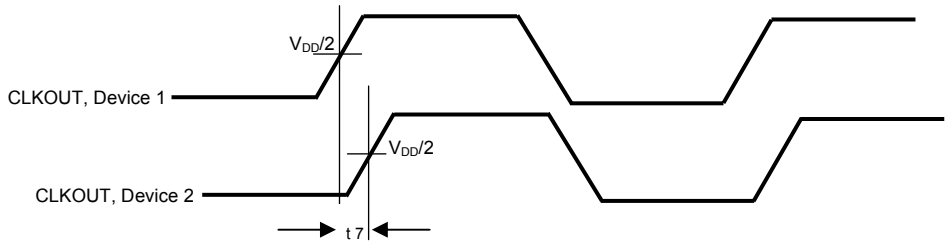
Output - Output Skew



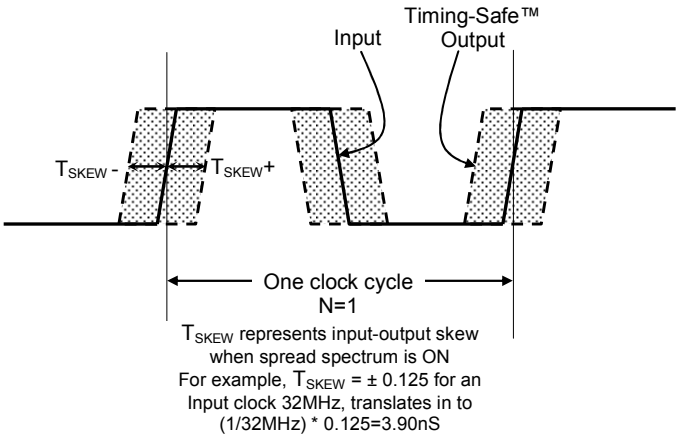
Input - Output Propagation Delay



Device - Device Skew

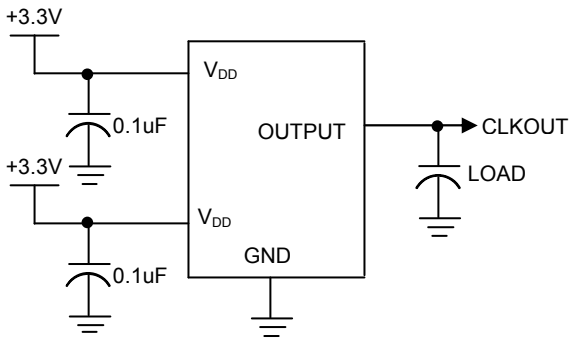


Input - Output Skew

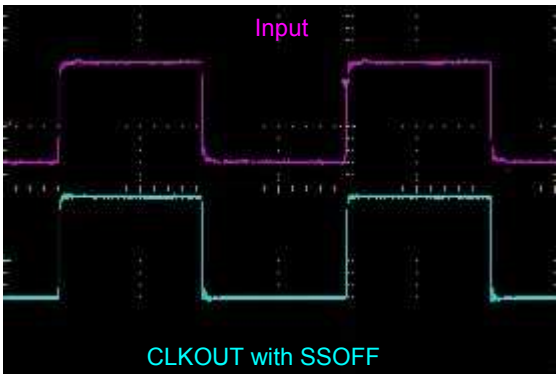


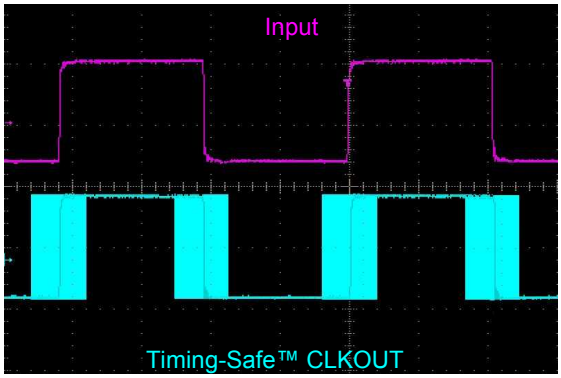
T_{SKEW} represents input-output skew when spread spectrum is ON
For example, T_{SKEW} = ± 0.125 for an Input clock 32MHz, translates in to (1/32MHz) * 0.125=3.90nS

Test Circuit



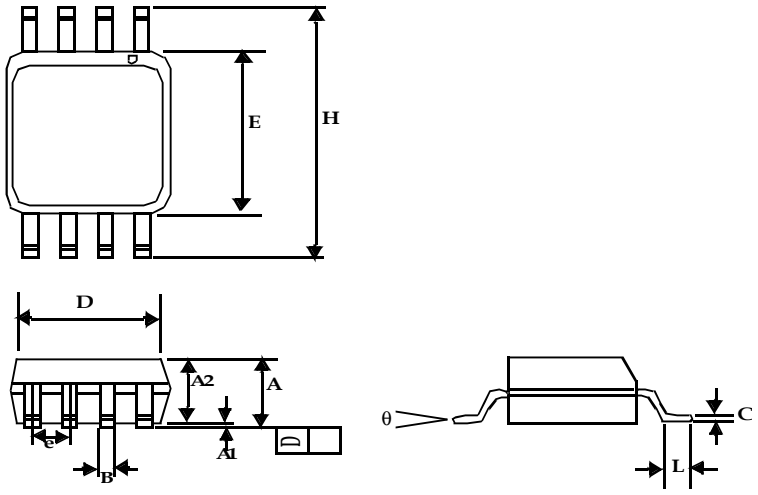
Typical example of Timing-Safe™ waveform





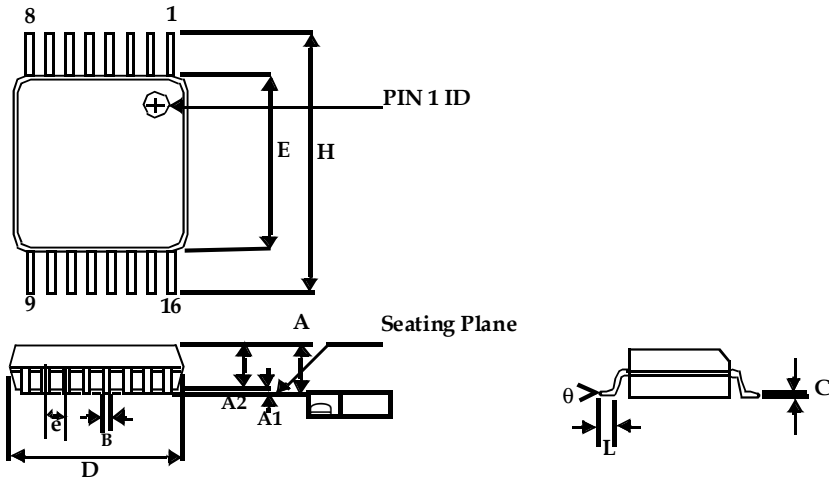
Package Information

8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

16-lead TSSOP (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
θ	0°	8°	0°	8°

Ordering Code

Ordering Code	Marking	Package Type	Temperature
P3P623S00BG-08SR	ADO	8-pin 150-mil SOIC-TAPE & REEL, Green	0℃ to +70℃
P3P623S00BG-08TR	ADO	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	0℃ to +70℃
P3I623S00BG-08TR	ADP	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	-40℃ to +85℃
P3P623S00EG-16TR	P623 S00E	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	0℃ to + 70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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