NVMe PCIe SSD
2.5” SSD
Manual

NVMe PCIe SSD is a non-volatile, solid-state storage device delivering uncompromising performance, reliability and ruggedness for environmentally challenging applications.

Revision History

Date	Revision	Description	Checked By
3/13/2017	A	Initial Release revised to new format from PSFN22xxxxWxxx_PM963_B. Add enterprise features. Update performance. Revise height to 14.8mm	
4/10/2017	B	Revise for 1725a by updating mechanical dimensions and performance. Revised all DC and AC characteristics, PBW, power, LBA, and environmental. Add UEFI EXPANSION ROM and VPD structure. Remove SPOR. Add Hot plug. Revised Supported Command Set.	
3/26/18	C	Remove SR-IOV info	

Legal Information

Legal Information

Ordering Information: 2.5 inch PCIe SSD Solid-State Drive

Part Numbers	Interface	Application	Useable Capacity (GB)[1]	Port	Temperature Range	NAND
VSFN25800GYCZWSE	PCIe/NVMe	Enterprise PM1725a	800 GB	Dual	(0 to +70'c)	Samsung TLC, V3 VNAND
VSFN251T60YCZWSE	PCIe/NVMe	Enterprise PM1725a	1600 GB	Dual	(0 to +70'c)	Samsung TLC V3 VNAND
VSFN253T20YCFWSM	PCIe/NVMe	Enterprise PM1725a	3200 GB	Dual	(0 to +70'c)	Samsung TLC V3 VNAND
VSFN256T40YCGWSM	PCIe/NVMe	Enterprise PM1725a	6400 GB	Dual	(0 to +70'c)	Samsung TLC V3 VNAND

Notes:

1. Usable capacity based on a level of over-provisioning applied to wear leveling, bad sectors, index tables etc.
2. SSD's ship unformatted from the factory unless otherwise requested.
3. 1 GB = 1,000,000,000 Byte
4. One Sector = 512 Byte.
5. SFF-8639 combo (SATA, SAS, PCIe) standard connector

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Product Picture(s)

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1 Introduction

Viking's 2.5 inch SSD presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe) 3.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe) Protocol.

The Viking's 2.5 inch SSD delivers wide bandwidth of up to 3300 MB/s for sequential read speed and up to 2950 MB/s for sequential write speed under 23W of power. With the help of Toggle 2.0 NAND Flash interface, the Viking's 2.5 inch SSD delivers random performance of up to 800K IOPS for random 4KB read and up to 160K IOPS for random 128KB write in the sustained state.

By combining the enhanced reliability of NAND Flash memory silicon with NAND Flash management technologies, the Viking's 2.5 inch SSD delivers the extended endurance suitable for enterprise applications, in 2.5 inch form factor.

In addition, the Viking's 2.5 inch SSD supports Power Loss Protection that can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure. Inrush current handler can protect the internal components from the electrical and physical damages.

1.1 Features

The SSD delivers the following features:

- Native-PCIe SSD for enterprise application
- LPDDR3 DRAM Buffer Memory
- PCI Express Gen3: Dual port X4 lanes
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVM Express Specification Rev.1.1a
- Enhanced Power-Loss Data Protection
- End-to-End Data Protection
- Support SSD Enhanced S.M.A.R.T. Feature Set
- Static and Dynamic Wear Leveling
- RoHS / Halogen-Free Compliant

1.2 PCIE Interface

- PCI Express Gen3:
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVM Express Specification Rev.1.1a

For a list of supported commands and other specifics, please see Chapter 5.

2 Product Specifications

2.1 Capacity and LBA count

User Capacity (GB)	Max LBA Count
800GB	1,562,824,367
1.6TB	3,125,627,567
3.2TB	6,251,233,967
6.4TB	12,502,446,767

Notes:

1. Per www.idema.org, LBA1-03 spec. The max. LBA shown in Table represents the total user addressable sectors in LBA mode and calculated by IDEMA rule.
   LBA counts = (97,696,368) + (1,953,504 * (Advertised Capacity in GBytes – 50))
2. Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes
3. Capacity shown in Tablerepresents the total usable capacity of the SSD which may be less than the total physical capacity. A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.

2.2 Performance

Table 2-1: Maximum Sustained Read and Write Bandwidth

Access Type	800 GB	1600 GB	3200 GB	6400 GB
Sequential Read, 256K, MB/s	Up to 3300	Up to 3300	Up to 3300	Up to 3300
Sequential Write, 256K, MB/s	Up to 1000	Up to 2200	Up to 3000	Up to 3300

Notes:

1. Based on PCI Express Gen3 x4, Random performance measured using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) with queue depth 32 by 4 workers and Sequential performance with queue depth 32 by 1 worker. Actual performance may vary depending on use conditions and environment.
2. Refer to Application Note AN0006 for Viking SSD Benchmarking Methodology.

Table 2-2: Maximum Random Read and Write Input/Output Operations per Second (IOPS)

Access Type	800 GB	1600 GB	3200 GB	6400 GB
Read, 4K, IOPS	Up to 700K	Up to 750K	Up to 800K	Up to 800K
Write, 4K, IOPS	Up to 70K	Up to 130K	Up to 160K	Up to 160K
Read, 8K, IOPS	Up to 390K	Up to 430K	Up to 430K	Up to 430K
Write, 8K, IOPS	Up to 36K	Up to 70K	Up to 95K	Up to 95K

Notes:

1. Based on PCI Express Gen3 x4, Random performance measured using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) with queue depth 32 by 4 workers and Sequential performance with queue depth 32 by 1 worker. Actual performance may vary depending on use conditions and environment.
2. Refer to Application Note AN0006 for Viking SSD Benchmarking Methodology

2.3 Timing / Latency

Table 2-3: Timing Specifications

Type (Queue Depth = 1)	800, 1600, 3200, 6400 GB
Random Read/Write Latency	90/30 µs
Sequential Read/Write Latency	115/125 µs
Power On Ready (POR), Drive Ready Time, 3840 GB	2 sec

Notes:

1. The random latency is measured by using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) and 4KB transfer size with queue depth 1 by 1 worker
2. The sequential latency is measured by using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) and 4KB transfer size with queue depth 1 by 1 worker

2.4 Quality of Service (QoS)

Table 2-4: Quality of Service (QoS)

Quality of Service (99%)	Unit	800GB	1.6TB	3.2TB	6.4TB
Read(4KB)(QD=1)	us	160	160	170	170
Write(4KB)(QD=1)	us	80	80	90	100
Read(4KB)(QD=128)	us	500	420	420	420
Write(4KB)(QD=128)	us	3500	2500	2500	2500
Quality of Service (99.99%)	**Unit**	**800GB**	**1.6TB**	**3.2TB**	**6.4TB**
Read(4KB)(QD=1)	us	180	180	300	300
Write(4KB)(QD=1)	us	150	250	500	500
Read(4KB)(QD=128)	us	780	550	570	570
Write(4KB)(QD=128)	us	7300	4000	4000	4000

Notes:

1. QoS is measured using Fio 2.1.3 (99 and 99.99%) in Linux RHEL 6.5 (Kernel 2.6.32) with queue depth 1, 32 on 4KB random read and write.
2. QoS is measured as the maximum round-trip time taken for 99 and 99.99% of commands to host

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Table 2-5: Operating Voltage IOPS Consistency

IOPS Consistency[1, 2]	Unit	800GB	1.6TB	3.2TB	6.4TB
Random Read (4 KB)	%	98	94	98	88
Random Write (4 KB)	%	90	88	92	98
Random Read (8 KB)	%	98	90	90	90
Random Write (8 KB)	%	90	90	90	90

NOTE:

1) IOPS consistency measured using FIO with queue depth 128.
2) IOPS Consistency (%) = (IOPS in the 99.9% slowest 1-second interval)/(average IOPS during the test).

2.5 Electrical Characteristics

2.5.1 Absolute Maximum Ratings

Values shown are stress ratings only. Functional operation outside normal operating values is not implied. Extended exposure to absolute maximum ratings may affect reliability.

2.5.2 Supply Voltage

The operating voltage is 12V

Table 2-6: Operating Voltage

Description	800GB/1.6/3.2/6.4TB
Operating Voltage	800GB/1.6/3.2/6.4TB
12V[2]	10%
12V Rise time (Max/Min)	50ms/1ms
12V Fall time (Max/Min)[4]	5s/1ms
12V Noise level	300 mV pp 10Hz – 100 KHz 50 mV pp 100KHz – 20 MHz
3.3Vaux[3]	10%
3.3Vaux Rise time (Max/Min)	50ms/1ms
3.3Vaux Fall time (Max/Min)[4]	5s/1ms
3.3Vaux Noise level	300 mV pp 10Hz – 100 KHz 50 mV pp 100KHz – 20 MHz

Notes:

1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system.
2) For 12V operating voltage, the minimum allowable is 10.8V and the maximum 13.2V.

2.5.3 Power Consumption

The SSD is implemented in standardized 2.5-inch form factor and gets primary 12V power as well as auxiliary 3.3V (3.3Vaux) power through the indicated pins (#P13~15 for 12V and #E3 for 3.3Vaux in SFF-8639 connector plug) from the host system.

Table 2-7: Typical Power Consumption at 12V

Power Mode		800GB	1.6TB	3.2TB	6.4TB
Active[2]	Read	16W	16W	16W	17W
	Write	15W	21W	21W	21W
Idle[3]	7.5W	7.5W	7.5W	7.5W	
Off	0W				

Notes:

1) Power consumption was measured in the 12V power pins (#P13~#P15) of the connector plug in SSD. The active and idle power is defined as the highest averaged power value, which is the maximum RMS average value over 100 ms duration.
2) The measurement condition for active power is assumed for 100% sequential read or write.
3) The idle state is defined as the state that the host system can issue any commands into SSD at any time.

Inrush Current	800GB/1.6/3.2/6.4TB
at 12V	1.8A[1]

Notes:

1) The measurement value of inrush current is also compatible with the standard specification of “Enterprise SSD Form Factor Version 1.0a” released by SSD Form Factor Working Group

2.6 Environmental Conditions

2.6.1 Temperature and Altitude

Table 2-8: Temperature and Altitude Related Specifications

Conditions	Operating	Shipping	Storage
Commercial Temperature- Case [1]	0 to 70°C	-40 to 85°C	-40 to 85°C
Humidity (non-condensing)	-	5 to 95%	5 to 95%

Notes:

1. Tc is measured at the surface of NAND Flash package

2.6.2 Shock and Vibration

SSD products are tested in accordance with environmental specification for shock and vibration.

Table 2-9: Shock and Vibration Specifications

		800GB/1.6/3.2/6.4TB
Shock[1]	Non-operating	1,500G
Vibration[2]	Non-operating	20 Gpeak (10~2,000Hz, Sweep sine)

NOTE:

1) Shock specifications assume that SSD shall be mounted with screws when input vibration is applied. Vibration may be applied in 3 axes (x, y and z) with a half sine waveform of 0.5ms duration in non-operating condition.
2) Vibration specifications assume that SSD shall be mounted with screws when input vibration is applied. The input vibration may be applied in 3 axes (x, y and z) and lasts during 15 minutes per axis.

2.6.3 Electromagnetic Immunity

2.5 inch is an embedded product for host systems and is designed not to impair with system functionality or hinder system EMI/FCC compliance.

2.7 Reliability

Table 2-10: Reliability Specifications

Parameter	Description			
Uncorrectable Bit Error Rate (UBER)	1 sector per 10^{17} bits read			
MTBF	2,000,000 hours			
Read Endurance	Unlimited			
Write Endurance (Petabytes Written)	**800GB**	**1600GB**	**3200GB**	**6400GB**
	7.3 PBW	14.6 PBW	29.2 TBW	58.4 TBW
Drive Write per day	5 DWPD over 5 years			
Data retention	> 90 days at NAND expiration			

Notes:
1. The reliability specification follows JEDEC standards JESD218A and JESD219A
2. TBW=(GB capacity x DWPD x 365 x years)/1000

2.8 Data Security

2.8.1 Power Loss Protection

By using internal back-up power technology, the Viking SSD supports power loss protection feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, the SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

2.9 Hot Plug Support

2.9.1 Power Loss Protection

By using internal back-up power technology, the Samsung SSD supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

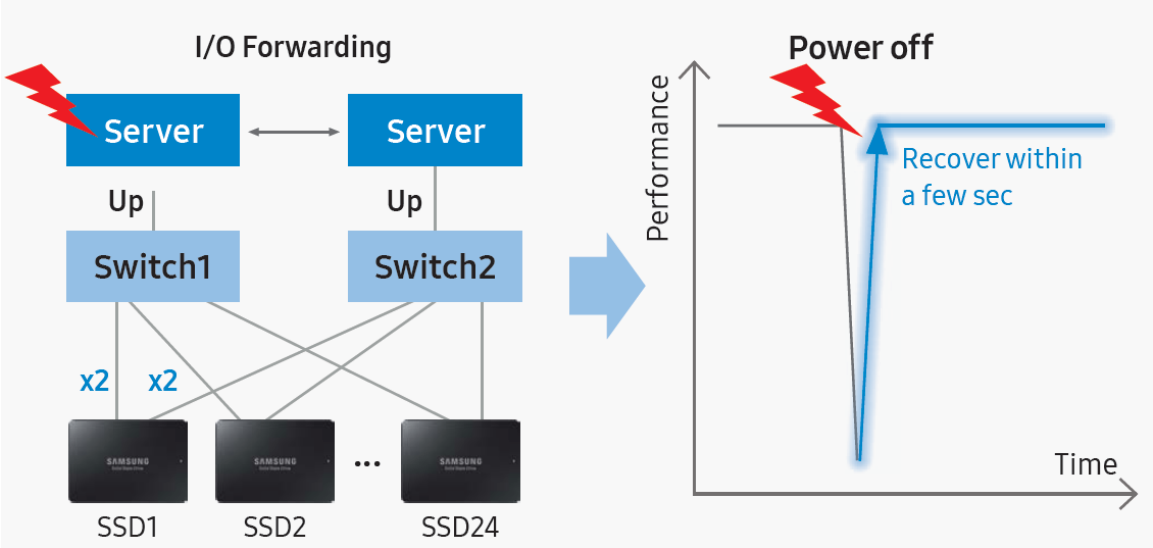
2.9.2 Inrush Current Protection

When the SSD plugs in the backplane of host system, the significant amount of current is induced through 12V power rail. The SSD has protection circuitry including a set of resisters and capacitors to alleviate the impact by inrush current through 12V power.

2.10 Enterprise Class Storage Features

2.10.1 Dual Port Capability

IT and data center managers need features that can provide access to storage data without interruptions. Viking has taken this need into consideration by including a key feature that provides access by smartly using dualport PCIe® (PCI Express®) SSDs to get the most out of highperformance enterprise applications. Viking has enabled this feature which provides the ability to create two fault domains and increases availability, providing non-interrupt service for accessing storage data. Even if a failure occurs in one of the paths to a port, preventing access along that path, the device is still accessible using the second port. The SSD provides virtually non-stop service with this dual-port feature support.



2.10.2 Multi-namespace support

The SSD supports multiple namespaces, where a single SSD can be partitioned into multiple hardware partitions. A namespace can be assigned to multiple hosts or dedicated to a single host. The SSD supports up to 32 multiple namespaces.

2.10.3 Remote Health Monitoring

This SSD provides a remote health-monitoring feature by an SSD Toolkit. The SSD Toolkit is a Samsung proprietary software designed to help users with easy-to-use SSD management and diagnostic features for server and data center usage.
The CLI (command line interface) tool currently supports NVMe SSDs and supports Linux®. The Samsung version of the SSD Toolkit is available from the Samsung SSD website at
http://www.samsung.com/global/business/semiconductor/minisite/SSD/global/html/support/server_downloads.html

Remote health monitoring features include:

- **Health monitoring:** Provides vital drive status information and supports users to update firmware, measure drive performance, initialize drives, calculate drive lifetime and more.

- **Remote health monitoring for FA (failure analysis):** Provides a smart way for resolving field issues by the remote health monitoring feature. This way of issue handling reduces turnaround time compared to the traditional way of handling the issue, such as dispatching an engineer, and provides quicker resolution.
  The customer can get the initial resolution in two steps: first by running the SSD Toolkit and second by sending the debug information back to the factory and getting the resolution effectively.

3 Mechanical Information

3.1 Dimensions

Table 3-1: Physical Dimensions

	Dimensions	Units
Height / Thickness	15.00+0.00, -0.50	mm
Width	69.85±0.25	mm
Length	100.20±0.25	mm

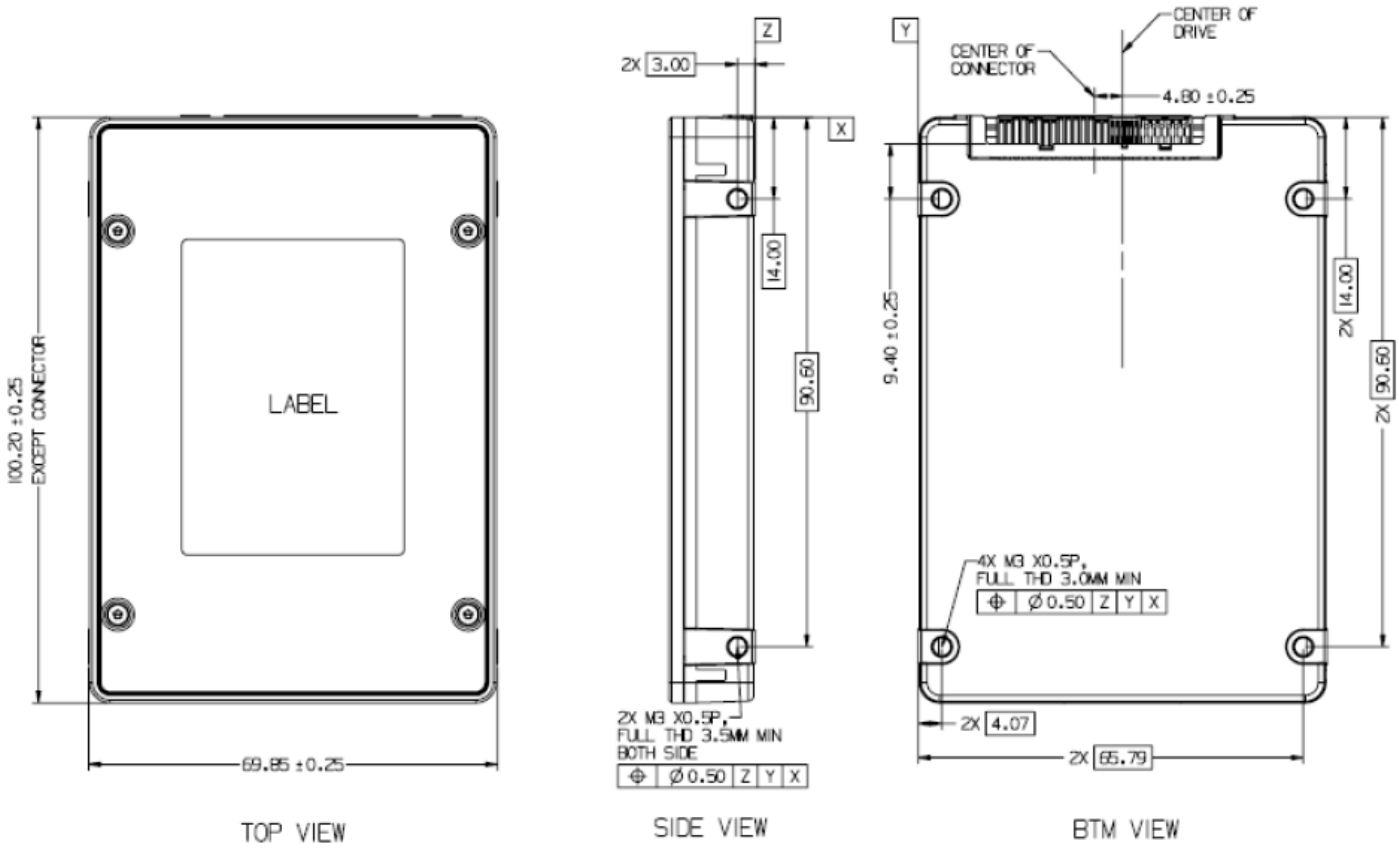


Figure 3-1: SDD Dimensions

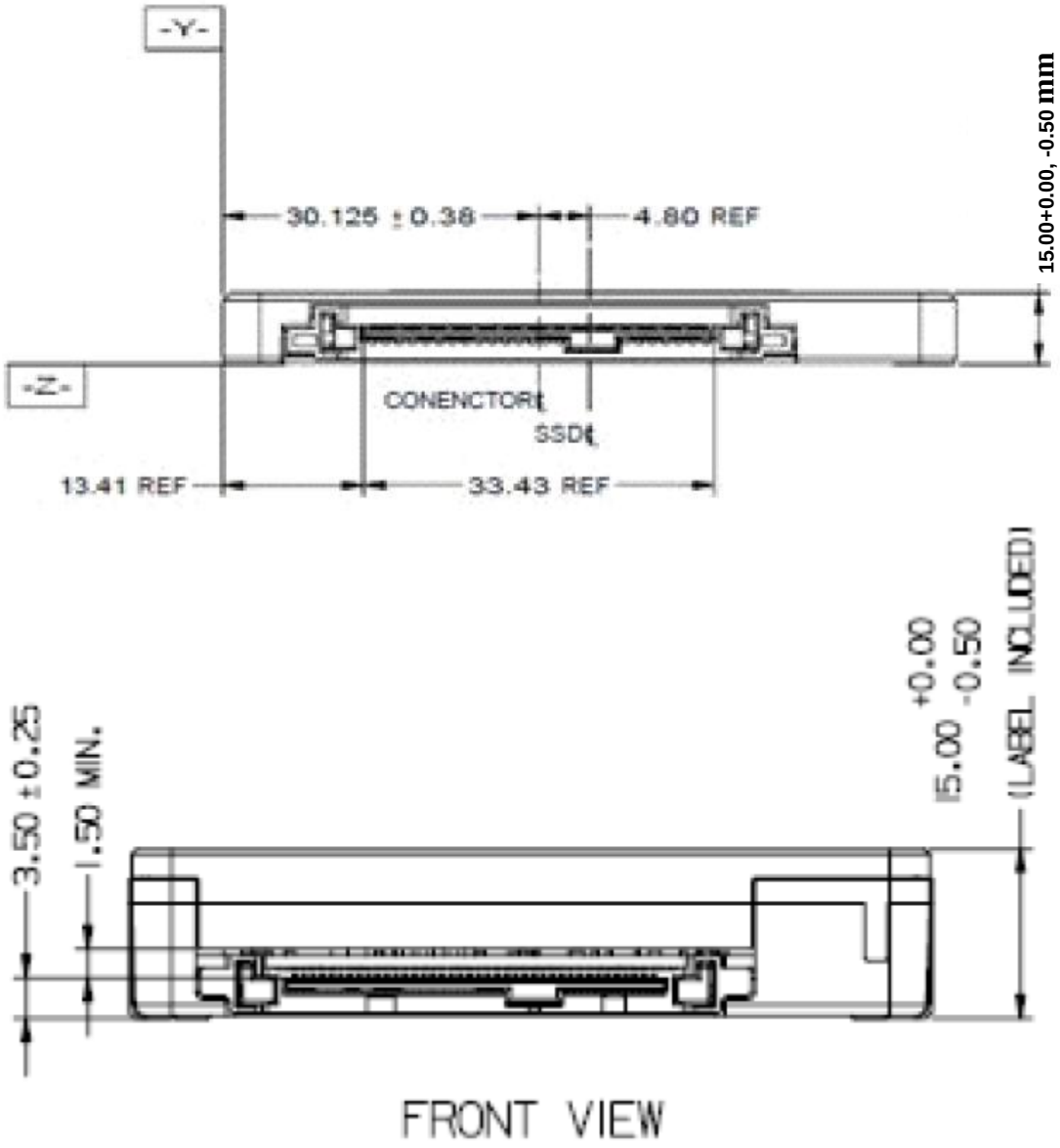
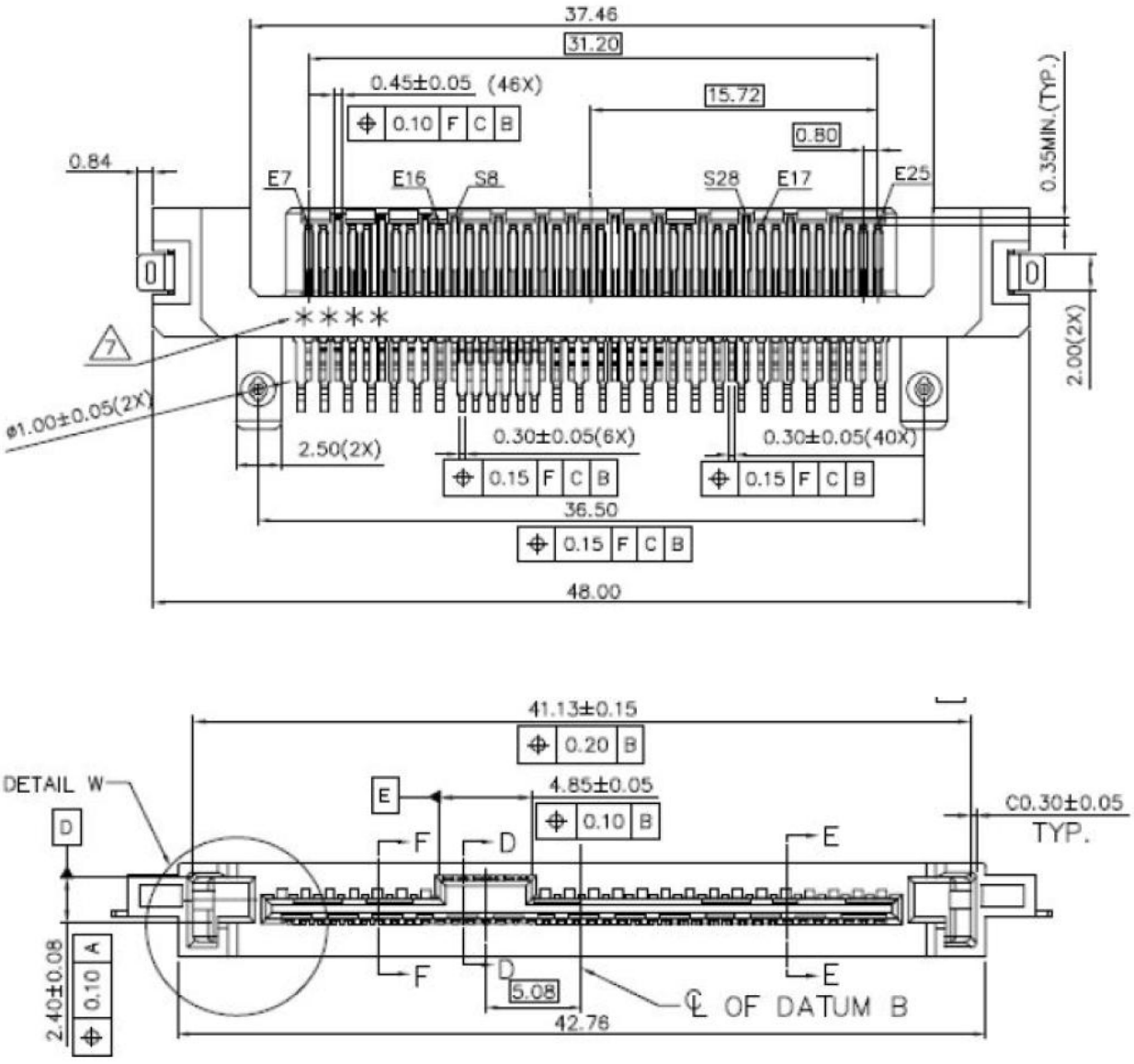


Figure 3-2: SDD Dimensions, Side View

Notes:

1. All dimensions are in millimeter. General tolerance is ± 0.15.



Note: SFF-8639 combo (SATA, SAS, PCIe) standard connector

Figure 3-3: Dimension Details for 2.5 inch connector

3.2 2.5 inch SSD Weight

Table 3-2: 2.5 inch SSD weight

Weight	Unit of measure
Up to 170g	Grams

4 Pin and Signal Descriptions

4.1 Signal and Power Description Tables

Table 4-1: 2.5 inch PCIE Connector Pinouts

Pin #	Assignment	Description	Pin #	Assignment	Description
S1	Not Used	Float	E7	RefClk0+	PCIe Reference Clock + (primary port A)
S2	Not Used		E8	RefClk0-	PCIe Reference Clock - (primary port A)
S3	Not Used		E9	GND	Ground
S4	Not Used	Ground	E10	PETp0	PCIe Transmit+ (lane 0)
S5	Not Used		E11	PETn0	PCIe Transmit- (lane 0)
S6	Not Used		E12	GND	Ground
S7	Not Used	Ground	E13	PERn0	PCIe Receive- (lane 0)
E1	REFCLK1+	PCIe Reference Clock + (dual port, port B)	E14	PERp0	PCIe Receive+ (lane 0)
E2	REFCLK1-	PCIe Reference Clock - (dual port, port B)	E15	GND	Ground
E3	3.3V AUX	Auxiliary Power (for SMBus access)	E16	Not Used	
E4	ePERST1#	PCIe Reset (dual port, port B)	S8	Not Used	Ground
E5	ePERST0#	PCIe Reset (primary port A)	S9	Not Used	
E6	Not Used		S10	Not Used	
P1	Not Used		S11	Not Used	Ground
P2	Not Used		S12	Not Used	
P3	Not Used		S13	Not Used	
P4	IfDet #	Interface Detect	S14	Not Used	Ground
P5	GND	Ground	S15	Not Used	
P6	GND	Ground	S16	GND	Ground
P7	Not Used		S17	PETp1	PCIe Transmit+ (lane 1)
P8	Not Used		S18	PETn1	PCIe Transmit- (lane 1)
P9	Not Used		S19	GND	Ground
P10	PRSNT #	Presence	S20	PERn1	PCIe Receive- (lane 1)

Pin #	Assignment	Description	Pin #	Assignment	Description
P11	Activity	Drive Active	S21	PERp1	PCIe Receive+ (lane 1)
P12	GND	Ground	S22	GND	Ground
P13	12 V	Primary Power	S23	PETp2	PCIe Transmit+ (lane 2)
P14	12 V	Primary Power	S24	PETn2	PCIe Transmit- (lane 2)
P15	12 V	Primary Power	S25	GND	Ground
			S26	PERn2	PCIe Receive- (lane 2)
			S27	PERp2	PCIe Receive+ (lane 2)
			S28	GND	Ground
			E17	PETp3	PCIe Transmit+ (lane 3)
			E18	PETn3	PCIe Transmit- (lane 3)
			E19	GND	Ground
			E20	PERn3	PCIe Receive- (lane 3)
			E21	PERp3	PCIe Receive+ (lane 3)
			E22	GND	Ground
			E23	SMClk	SMBus Clock
			E24	SMDat	SMBus Data
			E25	DualPortEn#	Dual Port PCIe enable

5 PCIe and NVM Express Registers

5.1 PCI Express Registers

5.1.1 PCI Register Summary

Table 5-1: PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
D0h	D4h	VPD Capability	PCI Capability
148h	157h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	17Bh	Secondary PCI Express Header	PCI Capability
188h	18Fh	Latency Tolerance Reporting (LTR)	PCI Capability
190h	19Fh	L1 Substates Capability Register	PCI Capability

5.1.2 PCI Header Registers

Table 5-2: PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test

Start Address	End Address	Symbol	Description
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

Table 5-3: Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A802h	Device ID
0:15	RO	144Dh	Vendor ID

Table 5-4: Command Register

Bits	Type	Default Value	Description
15:11	RO	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable (N/A)
7	RO	0	Zero value
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

Table 5-5: Device Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	N/A
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort
10:9	RO	0	N/A
8	RW1C	0	Master Data Parity Error Detected
7	RO	0	N/A
6	RO	0	Reserved
5	RO	0	N/A
4	RO	1	Capabilities List
3	RO	0	INTx Status
2:0	RO	0	Reserved

Table 5-6: Revision ID Register

Bits	Type	Default Value	Description
7:00	RO	1	Controller Hardware Revision ID

Table 5-7: Class Code Register

Bits	Type	Default Value	Description
23:16	RO	1h	Base Class Code
15:08	RO	8h	Sub Class Code
7:00	RO	2h	Programming Interface

Table 5-8: Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0h	N/A

Table 5-9: Master Latency Timer Register

Bits	Type	Default Value	Description
7:00	RO	0	N/A

Table 5-10: Header Type Register

Bits	Type	Default Value	Description
7:00	RO	0	N/A

Table 5-11: Built-in Self Test Register

Bits	Type	Default Value	Description
7:00	RO	0	N/A

Table 5-12: Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:04	RW	0	Base Address
3	RO	0	Pre-Fetchable
2:1	RO	2	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

Table 5-13: Memory Register Base Address Upper 32-bits (BAR1) Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-14: Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-15: BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-16: Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-17: Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-18: Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A801	Subsystem ID
15:0	RO	144D	Subsystem Vendor ID

Table 5-19: Expansion ROM Register

Bits	Type	Default Value	Description
31:11	RW	0	Expansion ROM Base Address
10:1	RO	0	Reserved
0	RW	0	Expansion ROM Enable/Disable

Table 5-20: Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer (Points to PCI Power Management Capability Offset)

Table 5-21: Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01	Interrupt Pin
7:0	RW	FF	Interrupt Line

Table 5-22: Minimum Grant Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-23: Maximum Latency Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

5.1.3 PCI Power Management Registers

Table 5-24: PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PID	PCI Power Management Capability ID
41h	41h	Next cap ptr	Next cap ptr
42h	43h	PMC	PC Power Management Capabilities
44h	45h	PMCS	PCI Power Management Control and Status
46h	46h	PMCSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	Data	Data

Table 5-25: PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:08	RO	50h	Next Capability
7:00	RO	1h	Capability ID

Table 5-26: PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0	N/A
10	RO	0	D2 Support
9	RO	0	D1 Support
8:6	RO	0	N/A
5	RO	0	Device Specific Initialization
4	RO	0	Reserved
3	RO	0	PME Clock
2:0	RO	3h	Version (Support for revision 1.2)

Table 5-27: PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RO	0	data register
23	RO	0	Bus power/Clock enable
22	RO	0	B2, B3 support
21:16	RsvdP	0	Reserved
15	RW1CS	0	PME Status
14:13	RO	0	N/A
12:09	RO	0	N/A
8	RWS	0	PME Enable
7:04	RsvdP	0	Reserved
3	RO	1	No Soft Reset
2	RsvdP	0	Reserved
1:00	RW	0	Power State

5.1.4 Message Signaled Interrupt Registers

Table 5-28: Message Signaled Interrupt Capability Register Summary

Start Address	End Address	Symbol	Description
50h	51h	MID	Message Signaled Interrupt Capability ID
52h	53h	MC	Message Signaled Interrupt Message Control
54h	57h	MA	Message Signaled Interrupt Message Address
58h	5Bh	MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MD	Message Signaled Interrupt Message Data
60h	63h	MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MPEND	Message Signaled Interrupt Pending Bits

Table 5-29: Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:08	RO	70h	Next Capability
7:0	RO	05h	Capability ID

Table 5-30: Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RsvdP	0	Reserved
8	RO	0	Per Vector Masking Capable
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	3h	Multiple Message Capable
0	RW	0h	MSI Enable

Table 5-31: Message Signaled Interrupt Lower Address Register

Bits	Type	Default Value	Description
31:2	RW	0	Address
1:0	RO	0	Reserved

Table 5-32: Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0	Upper Address

Table 5-33: Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
16:31	RsvdP	0	Reserved
0:15	RO	0	Data

Table 5-34: Message Signaled Interrupt Masked Bits Register

Bits	Type	Default Value	Description
31:0	RW	0	Mask Bits

Table 5-35: Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0	Pending Bits

5.1.5 MSI-X Registers

Table 5-36: MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MXID	MSI-X Capability ID
B2h	B3h	MXC	MSI-X Message Control
B4h	B7h	MTAB	MSI-X Table Offset and Table BIR
B8h	BBh	MPBA	MSI-X PBA Offset and PBA BIR

Table 5-37: MSI-X Identifier Register

Bits	Type	Default Value	Description
15:8	RO	00h	Next Capability
7:0	RO	11h	Capability ID

Table 5-38: MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RsvdP	0	Reserved
10:0	RO	08h	Table Size

Table 5-39: MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	300h	Table Offset
2:0	RO	0	Table BIR

Table 5-40: MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	200h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

5.1.6 PCI Express Capability Registers

Table 5-41: PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PXID	PCI Express Capability ID
72h	73h	PXCAP	PCI Express Capabilities
74h	77h	PXDCAP	PCI Express Device Capabilities
78h	79h	PXDC	PCI Express Device Control
7Ah	7Bh	PXDS	PCI Express Device Status
7Ch	7Fh	PXLCAP	PCI Express Link Capabilities
80h	81h	PXLC	PCI Express Link Control
82h	83h	PXLS	PCI Express Link Status
94h	97h	PXDCAP2	PCI Express Device Capabilities 2
98h	99h	PXDC2	PCI Express Device Control 2
9Ah	9Bh	PXDS2	PCI Express Device Status 2
9Ch	9Fh	PXLCAP2	PCI Express Link Capabilities 2
A0h	A1h	PXLC2	PCI Express Link Control 2
A2h	A3h	PXLS2	PCI Express Link Status 2

Table 5-42: PCI Express Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Pointer (MSI-X Capability)
7:0	RO	10h	Capability ID

Table 5-43: PCI Express Capabilities Register

Bits	Type	Default Value	Description
15:14	RsvdP	0	Reserved
13:9	RO	0	Interrupt Message Number
8	HwInit	0	N/A
7:4	RO	0	Device/Port Type
3:0	RO	2h	Capability Version

Table 5-44: PCI Express Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0	Reserved
28	RO	1	Function Level Reset Capability
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	0	Captured Slot Power Limit Value
17:16	RO	0	Reserved
15	RO	1	Role-based Error Reporting
14:12	RO	0	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0	Extended Tag Field Supported
4:3	RO	0	Phantom Functions Supported
2:0	RO	0	Max Payload Size Supported (128 byte payload)

Table 5-45: PCI Express Device Control Register

Bits	Type	Default Value	Description
15	RW	0	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1	Enable No Snoop
10	RWS	0	Aux Power PM Enable (N/A)
9	RW	0	Phantom Functions Enable (N/A)
8	RW	0	Extended Tag Enable
7:5	RW	0	Max Payload Size
4	RW	1	Enable Relaxed Ordering (N/A)
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

Table 5-46: PCI Express Device Status Register

Bits	Type	Default Value	Description
15:06	RsvdP	0	Reserved
5	RO	0	Transactions Pending
4	RO	1	Aux Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

Table 5-47: PCI Express Device Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HwInit	0 (Port 0)	Port Number
23	RsvdP	0	Reserved
22	HwInit	1h	ASPM Optionality Compliance
21	RO	0	Link Bandwidth Notification Capability (N/A)
20	RO	0	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0	Surprise Down Error Reporting Capable (N/A)
18	RO	1	Clock Power Management
17:15	RO	6	L1 Exit Latency
14:12	RO	6h	L0s Exit Latency
11:10	RO	0	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	3h	Supported Link Speeds

Table 5-48: PCI Express Device Link Control Register

Bits	Type	Default Value	Description
15:12	RsvdP	0	Reserved
11	RsvdP	0	Link Autonomous Bandwidth Interrupt Enable
10	RsvdP	0	Link Bandwidth Management Interrupt Enable
9	RsvdP	0	Hardware Autonomous Width Disable
8	RW	0	Enable Clock Power Management (N/A)
7	RW	0	Extended Sync
6	RW	0	Common Clock Configuration
5	RsvdP	0	Retrain Link
4	RsvdP	0	Link Disable
3	Root Ports (RO) End Points & Bridges (RW) Switch Ports (RO)	0	Read Completion Boundary (N/A)
2	RsvdP	0	Reserved
1:00	RW1C	0	Active State Power Management Control

Table 5-49: PCI Express Device Link Status Register

Bits	Type	Default Value	Description
15	RW1C	0h	Link Autonomous Bandwidth Status
14	RW1C	0	Link Bandwidth Management Status
13	RO	0	Data Link Layer Link Active
12	HwInit	1	Slot Clock Configuration
11	RO	0	Link Training (1: Link training in progress;0: No link training in progress) (Non-standard)
10	RO	0	Reserved
9:4	RO	4h	Negotiated Link Width
3:0	RO	3h	Current Link Speed

Table 5-50: PCI Express Device Capabilities 2 Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	Reserved
23:22	HwInit	0	Max End-End TLP Prefixes (N/A)
21	HwInit	0	End-End TLP Prefix Supported (N/A)
20	RO	0	Extended Format Field Supported (N/A)
19:18	HwInit	0	OBFF Supported (N/A)
17:14	RO	0	Reserved
13:12	RO	0	TPH Completer Supported (N/A)
11	RO	1	Latency Tolerance Reporting Supported (N/A)
10	HwInit	0	No RO-enabled PR-PR Passing (N/A)
9	RO	0	128-bit CAS Completer Supported (N/A)
8	RO	0	64-bit Atomic Op Completer Supported (N/A)
7	RO	0	32-bit Atomic Op Completer Supported (N/A)
6	RO	0	Atomic Op Routing Supported (N/A)
5	RO	0	ARI Forwarding Supported (N/A)
4	RO	1	Completion Timeout Disable Supported
3:0	HwInit	0	Completion Timeout Ranges Supported (50us to 200ms)

Table 5-51: PCI Express Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0	End-to-end TLP Prefix Blocking (N/A)
14:13	RW/RsvdP	0	OBFF Enable (N/A)
12:11	RsvdP	0	Reserved
10	RW/RsvdP	0	Latency Tolerance Reporting Mechanism Enable (N/A)
9	RW	0	IDO Completion Enable
8	RW	0	IDO Request Enable
7	RW	0	AtomicOp Egress Blocking
6	RW	0	AtomicOp Requester Enable
5	RW	0	ARI Forwarding Enable
4	RW	0	Completion Timeout Disable
3:0	RW	0	Completion Timeout Value (0h - 50 ȝs; 1h - 100 ȝs; 2h - 2 ms; 5h - 50 ms; 6h - 200 ms; others - reserved)

Table 5-52: PCI Express Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0	Reserved

Table 5-53: PCI Express Link Capabilities 2 Register

Bits	Type	Default Value	Description
31:9	RsvdP	0	Reserved
8	RO	0	Cross-Link Supported (N/A)
7:1	RO	7h	Supported Link Speeds 001b: 2.5 GT/s (Gen 1) 010b: 5.0 GT/s (Gen 2) 100b: 8 GT/s (Gen 3)
0	RsvdP	0	Reserved

Table 5-54: PCI Express Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0	Compliance De-emphasis
11	RWS/RsvdP	0	Compliance SOS
10	RWS/RsvdP	0	Enter Modified Compliance
9:7	RWS/RsvdP	0	Transmit Margin
6	HwInit	0	Select De-Emphasis
5	RWS/RsvdP	0	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0	Enter Compliance
3:0	RWS/RsvdP	3h	Target Link Speed 1h: 2.5 GT/s (Gen 1) 2h: 5.0 GT/s (Gen 2) 3h: 8 GT/s (Gen 3)

Table 5-55: PCI Express Link Status 2 Register

Bits	Type	Default Value	Description
15:6	RsvdP	0	Reserved
5	RW1CS	0	Link Equalization Request
4	ROS	0	Equalization Phase 3 Successful
3	ROS	0	Equalization Phase 2 Successful
2	ROS	0	Equalization Phase 1 Successful
1	ROS	0	Equalization Complete
0	RO	1	Current De-Emphasis

5.1.7 Advanced Error Reporting Registers

Table 5-56: Advanced Error Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
100h	103h	AERID	AER Capability ID
104h	107h	AERUCES	AER Uncorrectable Error Status
108h	10Bh	AERUCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AERUCESEV	AER Uncorrectable Error Severity
110h	113h	AERCES	AER Correctable Error Status
114h	117h	AERCEM	AER Correctable Error Mask
118h	11Bh	AERCC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AERHL	AER Header Log

Table 5-57: AER Capability ID Register

Bits	Type	Default Value	Description
31:20:00	RO	148h	Next Pointer (Points to Secondary PCI Express Extended Capability Header Offset)
19:16	RO	2h	Capability Version
15:00	RO	1h	Capability ID

Table 5-58: AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:26	RsvdZ	0	Reserved
25	RsvdZ	0	TLP Prefix Blocked Error Status (N/A)
24	RsvdZ	0	Atomic Op Egress Blocked Status (N/A)
23	RsvdZ	0	Reserved
22	RW1CS	0	Uncorrectable Internal Error Status
21	RsvdZ	0	Reserved
20	RW1CS	0	Unsupported Request Error Status
19	RW1CS	0	ECRC Error Status
18	RW1CS	0	Malformed TLP Status
17	RW1CS	0	Receiver Overflow Status (N/A)
16	RW1CS	0	Unexpected Completion Status
15	RW1CS	0	Completer Abort Status
14	RW1CS	0	Completion Timeout Status
13	RW1CS	0	Flow Control Protocol Error Status (N/A)
12	RW1CS	0	Poisoned TLP Status
11:6	RsvdZ	0	Reserved
5	RsvdZ	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status
3:1	RsvdP		Reserved
0	Undefined	0	Undefined

Table 5-59: AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:26	RsvdZ	0	Reserved
25	RsvdZ	0	TLP Prefix Blocked Error Mask (N/A)
24	RsvdZ	0	Atomic Op Egress Blocked Mask (N/A)
23	RsvdZ	0	MC Blocked TLP Mask (N/A)
22	RWS	1	Uncorrectable Internal Error Mask
21	RsvdZ	0	ACS Violation Mask (N/A)
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver Overflow Mask (N/A)
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask
13	RWS	0	Flow Control Protocol Error Mask (N/A)
12	RWS	0	Poisoned TLP Mask
11:6	RsvdP	0	Reserved
5	RsvdZ	0	Reserved
4	RWS	0	Data Link Protocol Error Mask
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

Table 5-60: AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:26	RsvdP	0	Reserved
25	RsvdP	0	TLP Prefix Blocked Error Mask (N/A)
24	RsvdP	0	Atomic Op Egress Blocked Mask (N/A)
23	RsvdP	0	Reserved
22	RWS	1	Uncorrectable Internal Error Mask
21	RsvdP	0	Reserved
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	1	Malformed TLP Mask
17	RWS	1	Receiver Overflow Mask (N/A)
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask
13	RWS	1	Flow Control Protocol Error Mask (N/A)
12	RWS	0	Poisoned TLP Mask
11:6	RsvdP	0	Reserved
5	RsvdP	1	Reserved
4	RWS	1	Data Link Protocol Error Mask
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

Table 5-61: AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0	Reserved
15	RsvdZ	0	Reserved
14	RW1CS	0	Corrected Internal Error Status (N/A)
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status
11:9	RsvdZ	0	Reserved
8	RW1CS	0	Replay Number Rollover Status
7	RW1CS	0	Bad DLLP Status
6	RW1CS	0	Bad TLP Status
5:1	RsvdZ	0	Reserved
0	RW1CS	0	Received Error Status

Table 5-62: AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15	RsvdP	0	Reserved
14	RWS	1	Corrected Internal Error Mask (N/A)
13	RWS	1	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask
11:9	RsvdP	0	Reserved
8	RWS	0	Replay Number Rollover Mask
7	RWS	0	Bad DLLP Mask
6	RWS	0	Bad TLP Mask
5:1	RsvdP	0	Reserved
0	RW	0	Received Error Mask

Table 5-63: AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:12	RsvdP	0	Reserved
11	RsvdP	0	TLP Prefix Log Present (N/A)
10	RsvdP	0	Reserved
9	RsvdP	0	Reserved
8	RWS	0	ECRC Check Enable
7	RO	1	ECRC Check Capable
6	RWS	0	ECRC Generation Enable
5	RO	1	ECRC Generation Capable
4:0	ROS	0	First Error Pointer

Table 5-64: AER Header Log Register

Bits	Type	Default Value	Description
0	ROS	0	Header Byte 3
1	ROS	0	Header Byte 2
2	ROS	0	Header Byte 1
3	ROS	0	Header Byte 0
4	ROS	0	Header Byte 7
5	ROS	0	Header Byte 6
6	ROS	0	Header Byte 5
7	ROS	0	Header Byte 4
8	ROS	0	Header Byte 11
9	ROS	0	Header Byte 10
10	ROS	0	Header Byte 9
11	ROS	0	Header Byte 8
12	ROS	0	Header Byte 15
13	ROS	0	Header Byte 14
14	ROS	0	Header Byte 13
15	ROS	0	Header Byte 12

Table 5-65: AER TLP Prefix Log Register

Bits	Type	Default Value	Description
0	RO	0	First TLP Prefix Log Byte 3 (N/A)
1	RO	0	First TLP Prefix Log Byte 2 (N/A)
2	RO	0	First TLP Prefix Log Byte 1 (N/A)
3	RO	0	First TLP Prefix Log Byte 0 (N/A)
4	RO	0	Second TLP Prefix Log Byte 7 (N/A)
5	RO	0	Second TLP Prefix Log Byte 6 (N/A)
6	RO	0	Second TLP Prefix Log Byte 5 (N/A)
7	RO	0	Second TLP Prefix Log Byte 4 (N/A)
8	RO	0	Third TLP Prefix Log Byte 11 (N/A)
9	RO	0	Third TLP Prefix Log Byte 10 (N/A)
10	RO	0	Third TLP Prefix Log Byte 9 (N/A)
11	RO	0	Third TLP Prefix Log Byte 8 (N/A)
12	RO	0	Fourth TLP Prefix Log Byte 15 (N/A)
13	RO	0	Fourth TLP Prefix Log Byte 14 (N/A)
14	RO	0	Fourth TLP Prefix Log Byte 13 (N/A)
15	RO	0	Fourth TLP Prefix Log Byte 12 (N/A)

Table 5-66: Secondary PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
168h	16Bh	SPXID	Secondary PCI Express Capability
16Ch	16Fh	PXLC3	PCI Express Link Control 3
170h	173h	PXLE	PCI Express Lane Error Status
174h	175h	PXL0EC	PCI Express Lane 0 Equalization Control
176h	177h	PXL1EC	PCI Express Lane 1 Equalization Control
178h	179h	PXL2EC	PCI Express Lane 2 Equalization Control
17Ah	17Bh	PXL3EC	PCI Express Lane 3 Equalization Control

Table 5-67: Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	188h	Next Pointer (Viking Vendor Specific Capability)
19:16	RO	1h	Capability Version
15:0	RO	0019h	Capability ID (Secondary PCI Express Extended capability)

Table 5-68: PCI Express Link Control 3 Register

Bits	Type	Default Value	Description
31:2	Rsvdp	0	Reserved
1	Rsvdp	0	Link Equalization Request Interrupt Enable (N/A)
0	Rsvdp	0	Perform Equalization (N/A)

Table 5-69: PCI Express Lane Error Status Register

Bits	Type	Default Value	Description
31:4	Rsvdp	0	Reserved
3:0	RW1CS	0	Lane Error Status Bits

Table 5-70: PCI Express Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

Table 5-71: PCI Express Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

Table 5-72: PCI Express Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

Table 5-73: PCI Express Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

5.1.8 Device Serial Number Capability Register

Table 5-74: Device Serial Number Capability Register Header

Bits	Type	Default Value	Description
31:20	RO	158h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	3h	PCI Express Extended Capability ID

Table 5-75: Serial Number Register Header (offset 0x4/0x8)

Bits	Type	Default Value	Description
31:0	RO	parameter	Serial Number register (1st dword)

5.1.9 Power Budgeting Extended Capability

Table 5-76: Power Budgeting Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	168h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	4h	PCI Express Extended Capability ID

Table 5-77: Data Register

Bits	Type	Default Value	Description
31:21	RsvdP	0	Reserved
20:18	RO	0	Power Rail
17:15	RO	0	Type
14:13	RO	0	PM State
12:10	RO	0	PM Sub State
9:8	RO	0	Data Scale
7:0	RO	0	Base Power

Table 5-78: Power Budget Capability Register

Bits	Type	Default Value	Description
7:1	RsvdP	0	Reserved
0	HwInit	0	System Allocated

5.1.10 Latency Tolerance Reporting Capability Registers

Table 5-79: LTR Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	188h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	18h	PCI Express Extended Capability ID

Table 5-80: LTR Max Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max Snoop latency Scale
9:0	RW	0	Max Snoop latency Value

Table 5-81: LTR Max No Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max No Snoop latency Scale
9:0	RW	0	Max No Snoop latency Value

5.1.11 L1 Substates Capability Registers

Table 5-82: L1 Substates Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	0	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	1Eh	PCI Express Extended Capability ID

Table 5-83: L1 Substates Capability Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	Reserved
23:19	HwInit	5h	Port Power on value
18	RsvdP	0	Reserved
17:16	HwInit	0	Port T_Power_on scale
15:8	HwInit	Ah	Port Common_mode_restore_time
7:5	RsvdP	0	Reserved
4	HwInit	0	L1 PM Substates Supported
3	HwInit	0	ASPM PM L1.1 Supported
2	HwInit	0	ASPM PM L1.2 Supported
1	HwInit	0	PCI PM L1.1 Supported
0	HwInit	0	PCI PM L1.2 Supported

Table 5-84: L1 Substates Control1 Register

Bits	Type	Default Value	Description
31:29	RW	0	LTR L1.2 Threshold Scale
28:26	RsvdP	0	Reserved
25:16	RW	0	LTR L1.2 Threshold value
15:8	RsvdP	0	Common_mode_restore_time
7:4	RsvdP	0	Reserved
3	RW	0	ASPM PM L1.1 Supported
2	RW	0	ASPM PM L1.2 Supported
1	RW	0	PCI PM L1.1 Supported
0	RW	0	PCI PM L1.2 Supported

Table 5-85: L1 Substates Control2 Register

Bits	Type	Default Value	Description
31:8	RsvdP	0	Reserved
7:3	RW	5	T_POWER_ON Value
2	RsvdP	0	Reserved
1:0	RW	0	T_POWER_ON Scale

5.2 NVM Express Registers

5.2.1 Register Summary

Table 5-86: Register Summary

Start Address	End Address	Symbol	Description
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	Reserved	Reserved
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
	...		
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDVL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

Table 5-87: Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56:00	RO		0h	Reserved
55:52:00	RO	MPSMAX	Fh	Memory Page Size Maximum (Maximum is 8KB)
51:48:00	RO	MPSMIN	0	Memory Page Size Minimum (Minimum is 4KB)
47:45:00	RO		0	Reserved
44:37:00	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO		0	Reserved
35:32:00	RO	DSTRD	0	Doorbell Stride 0: Stride of 4 bytes
31:24:00	RO	TO	3Ch	Timeout 4h: 2 seconds
23:19	RO		0	Reserved
18:17	RO	AMS	0	Arbitration Mechanism Supported (Only support round robin)
16	RO	CQR	1	Contiguous Queues Required
15:00	RO	MQES	3FFFh	Maximum Queue Entries Supported (16384 entries supported)

Table 5-88: Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:0	RO	MNR	100h	Minor Version Number

Table 5-89: Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:00	RW1S	IVMS	0	Interrupt Vector Mask Set

Table 5-90: Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	0	Interrupt Vector Mask Clear

Table 5-91: Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0	Reserved
23:20	RW	IOCQES	0	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	0	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0	Reserved
0	RW	EN	0	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

Table 5-92: Controller Status

Bits	Type	Name	Default Value	Description
31:4	RO	-	0	Reserved
3:2	RO	SHST	0	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0	Controller Fatal Status
0	RO	RDY	0	1h: Controller ready to process commands 0h: Controller shall not process commands.

Table 5-93: Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0	Reserved
27:16	RW	ACQS	0	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0	Reserved
11:0	RW	ASQS	0	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

Table 5-94: Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0	Admin Submission Queue Base Address
11:0	RO	-	0	Reserved

Table 5-95: Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0	Admin Completion Queue Base Address
11:0	RO	-	0	Reserved

Table 5-96: Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	SQT	0	Submission Queue Tail

Table 5-97: Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	CQH	0	Completion Queue Head

6 Supported Command Set

6.1 Admin Command Set

Table 6-1: Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page - Error Information (01h) - SMART/Health Information (02h) - Firmware Slot Information (03h, M)
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature - Arbitration (01h) - Power Management (02h) - LBA Range Type (03h) - Temperature Threshold (04h) - Error Recovery (05h) - Number of Queues (07h) - Interrupt Coalescing (08h) - Interrupt Vector Configuration (09h) - Write Atomicity (0Ah) - Asynchronous Event Configuration (0Bh) - Software Progress Marker (80h)
0Ah	Get Feature - Arbitration (01h) - LBA Range Type (03h) - Temperature Threshold (04h) - Error Recovery (05h) - Number of Queues (07h) - Interrupt Coalescing (08h) - Interrupt Vector Configuration (09h) - Write Atomicity (0Ah) - Asynchronous Event Configuration (0Bh) - Software Progress Marker (80h)
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
15h	Namespace Attachment
80h	Format NVM
81h – BFh	I/O Command Set Specific

6.1.1 Identify Command

Table 6-2: Identify Controller Data Structure

Bytes	O/M	Default Value	Description
Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	144Dh	PCI Subsystem Vendor ID
23:4	M	SXXXNXXXXXXXXX	Serial Number (ASCII), X: Variables
63:24	M	800GB : SAMSUNG MZWLL800HEHP-00003 1.6TB : SAMSUNG MZWLL1T6HEHP-00003 3.2TB : SAMSUNG MZWLL3T2HMJP-00003 6.4TB : SAMSUNG MZWLL6T4HMLS-00003	Model Number (ASCII)
71:64	M	GPNAXB3Q	Firmware Revision, X: Variables
72	M	8h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI Byte 73 - 38h Byte 74 - 25h Byte 75 - 0h
76	O	3h	Multi-Interface Capabilities 0h: Not supported (single port) 1h: Supported (dual port – future value)
77	M	5h	Maximum Data Transfer Size 0h: No restrictions
79:78	M	21h	Controller ID (CNTLID)
83:80	M	10200h	Version (VER)
87:84	M	E4E1C0h	RTD3 Resume Latency (RTD3R)
91:88	M	989680h	RTD3 Entry Latency (RTD3E)
95:92	M	300h	Optional Asynchronous Event Supported (OAES)
239:96		-	Reserved
255:240		Refer to the NVMe Management Interface Specification for definition.	
257:256	M	0Eh	Optional Admin Command Support Bits 15:3 - Reserved Bit 3: Namespace Management and Namespace Attachment command Supported Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported (TBD)
258	M	7h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	Fh	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	17h	Firmware Updates Bits 7:4 – Reserved Bits 3:1 – Number of firmware slots Bit 0 – 1h Slot 1 is read only

Bytes	O/M	Default Value	Description
261	M	2h	Log Page Attributes Bits 7:1 – Reserved Bit 0: 0h SMART data is global for all Namespaces
262	M	FFh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)
263	M	0h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.1b Figure 8.
265	O	0h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	15Fh	Warning Composite Temperature Threshold (WCTEMP)
269:268	M	166h	Critical Composite Temperature Threshold (CCTEMP)
271:270	O	78h	Maximum Time for Firmware Activation (MTFA)
275:272	O	0h	Host Memory Buffer Preferred Size (HMPRE):
279:276	O	0h	Host Memory Buffer Minimum Size (HMMIN):
295:280	O	800GB : BA4D9D6000 1.6TB : 1749A956000 3.2TB : 2E934856000 6.4TB : 5D268656000	Total NVM Capacity (TNVMCAP):
311:296	O	0h	Unallocated NVM Capacity (UNVMCAP):
315:312	O	0h	Replay Protected Memory Block Support (RPMBS):
511:316	-	-	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)
515:514	-	-	Reserved
519:516	M	20h	Number of Namespaces
521:520	M	3Eh	Optional NVM Command Support Bits 51:3 – Reserved Bit 2 – 1h Dataset Management Supported Bit 1 – 0h Write Uncorrectable Supported Bit 0 – 0h Compare Not Supported
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	4h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase is applied for All Namespaces Bit 0 – 0h Format Per Namespace
525	M	0h	Volatile Write Cache 0h – No VWC present
527:526	M	FFFFh	Atomic Write Unit Normal All commands atomic
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 –

Bytes	O/M	Default Value	Description
			Indicates NVM Vendor Specific Commands use the format defined in NVM Express 1.2 Figure 8.
531	M	-	Reserved
533:532	O	0h	Atomic Compare & Write Unit (ACWU)
535:534	M	-	Reserved
539:536	O	70001h	SGL Support (SGLS)
703:540	M	-	Reserved
I/O Command Set Attributes			
2047:704	-	-	Reserved
Power State Descriptors			
2079:2048	M	-	Power State 0 Descriptor
2111:2080	O	-	Power State 1 Descriptor (N/A)
…	-		
3071:3040	O	-	Power State 31 Descriptor (N/A)
4095:3072	-	0h	Samsung Reserved

Table 6-3: Identify Power State Descriptor Data Structure

Bits	Power State 0	Description
255:125	0	Reserved
124:120	0	Relative Write Latency
119:117	0	Reserved
116:112	0	Relative Write Throughput
111:109	0	Reserved
108:104	0	Relative Read Latency
103:101	0	Reserved
100:96	0	Relative Read Throughput
95:64	100	Exit Latency (100us)
63:32	100	Entry Latency (100us)
31:16	0	Reserved
15:00	09C4h	Maximum Power (25W)

Table 6-4: Identify Namespace Data Structure

Bytes	O/M	Default Value	Description
7:00	M	800GB : 5D26CEB0 (512B),BA4D9D6 (4096) 1.6TB: BA4D4AB0 (512B),1749A956 (4096) 3.2TB: 1749A42B0 (512B),2E934856 (4096) 6.4TB: 2E93432B0 (512B),5D268656 (4096))	Namespace Size
15:88	M	800GB : 5D26CEB0 (512B),BA4D9D6 (4096) 1.6TB: BA4D4AB0 (512B),1749A956 (4096) 3.2TB: 1749A42B0 (512B),2E934856 (4096) 6.4TB: 2E93432B0 (512B),5D268656 (4096)	Namespace Capacity
23:16	M	800GB : 5D26CEB0 (512B),BA4D9D6 (4096) 1.6TB: BA4D4AB0 (512B),1749A956 (4096) 3.2TB: 1749A42B0 (512B),2E934856 (4096) 6.4TB: 2E93432B0 (512B),5D268656 (4096)	Namespace Utilization A device may report Namespace Utilization equal to Namespace Capacity at all times if the product is not targeted for thin provisioning environments
24	M	0h	Namespace Features Bits 7:1 Reserved Bit 0: Thin provisioning not supported
25	M	3h	Number of LBA Formats
26	M	10h	Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	3h	Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA

Bytes	O/M	Default Value	Description
28	M	1Fh	End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
29	M	0h	End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30	O	1h	Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1 : Accessible by two or more controllers Bit 0 - 0 : Private namespace
31	O	7h	Reservation Capabilities (RESCAP) Bits 7 - Reserved Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5 - 1 : Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4 - 1 : Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3 - 1 : Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2 - 1 : Namespace supports the Exclusive Access Reservation type Bit 1 - 1 : Namespace supports the Write Exclusive Reservation type Bit 0 - 1 : Namespace supports the Persist Through Power Loss capability
32	O	80h	Format Progress Indicator (FPI)
33	-	-	Reserved
35:34	O	0h	Namespace Atomic Write Unit Normal (NAWUN)
37:36	O	0h	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	O	0h	Namespace Atomic Compare & Write Unit (NACWU)
41:40	O	0h	Namespace Atomic Boundary Size Normal (NABSN)
43:42	O	0h	Namespace Atomic Boundary Offset (NABO)
45:44	O	0h	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	-	-	Reserved
63:48	O	800GB : BA4D9D6000 1.6TB : 1749A956000 3.2TB : 2E934856000 6.4TB : 5D268656000	NVM Capacity (NVMCAP)
103:64	-	-	Reserved
119:104	O	Device Dependant	Namespace Globally Unique Identifier (NGUID)
127:120	O	TBD	IEEE Extended Unique Identifier(EUI64)
131:128	M	1090000h	LBA Format 0 Support
135:132	O	3090008h	LBA Format 1 Support
139:136	O	C0000h	LBA Format 2 Support
143:140	O	20C0008h	LBA Format 3 Support
147:144	O	-	LBA Format 4 Support (N/A)

Bytes	O/M	Default Value	Description
…			
191:188	O	-	LBA Format 15 Support (N/A)
383:192	-	-	Reserved
Vendor Specific			
4095:384	-	-	Samsung Reserved

Table 6-5: LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26		0h	Reserved
25:24	RP	1h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0h	Metadata Size

Table 6-6: LBA Format 1 Data Structure

Bits	Name	Default Value	Description
31:26		0h	Reserved
25:24	RP	3h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	8h	Metadata Size

Table 6-7: LBA Format 2 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	0h	Metadata Size

Table 6-8: LBA Format 3 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	2h	Relative Performance
23:16	LBADS	Ch	LBA Data Size (2^n bytes)
15:00	MS	8h	Metadata Size (bytes)

6.2 NVM Express I/O Command Set

Table 6-9: Opcode for NVM Express I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write

02h	Read
09h	Dataset Management
0Dh	Reservation Register
0Eh	Reservation Report
11h	Reservation Acquire
15h	Reservation Release
04h	Write Uncorrectable[1]
05h	Compare [1]
08h	Write Zeroes[1]

Notes
1) Optional

6.3 SMART/Health Information

Table 6-10: SMART/Health Information Log

Bytes	Default Value	Attribute Description
0	0	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the device reliability has been degraded due to significant media related errors or any internal error that degrades device reliability Bit 1 – 1h: the temperature has exceeded a critical threshold Bit 0 – 1h: the available spare space has fallen below the threshold
2:1	Temperature	Temperature
3	100	Available Spare
4	10	Available Spare Threshold
5	0	Percentage Used
31:6	-	Reserved
47:32	0	Data Units Read
63:48	0	Data Units Written
79:64	0	Host Read Commands
95:80	0	Host Write Commands
111:96	0	Controller Busy Time
127:112	0	Power Cycles
143:128	0	Power On Hours
159:144	0	Unsafe Shutdowns
175:160	0	Media Errors
191:176	0	Number of Error Information Log Entries
511:192	-	Reserved
195:192	0	Warning Composite Temperature Time
199:196	0	Critical Composite Temperature Time
201:200	0	Temperature Sensor 1
203:202	0	Temperature Sensor 2
	0	Temperature Sensor 3

Bytes	Default Value	Attribute Description
205:204		
207:206	0	Temperature Sensor 4 (N/A)
209:208	0	Temperature Sensor 5 (N/A)
211:210	0	Temperature Sensor 6 (N/A)
213:212	0	Temperature Sensor 7 (N/A)
215:213	0	Temperature Sensor 8 (N/A)
511:216	-	Reserved

7 SFF-8639 SMBus RESOURCES

This section listed data structures and registers accessible through SMBus interface. Vital Product Data (VPD) is stored in SM-Bus slave address of 0xA6 (bits 7-1 correspond to 1010_011 on the SM-Bus). Temperature sensor is stored in SM-Bus slave address of 0xD4 (bits 7-1 correspond to 1101_010).

7.1 Vital Product Data (VPD) Structure

VPD listed device specific information for Enterprise PCIe SSD discovery and power allocation.

Table 7-1: Vital Product Data (VPD) Structure

Bytes	Name	Default Value	Description
02:00	Class Code	010802h	Device Type & Programming Interface
04:03	ID	144Dh	PCI-SIG Vendor ID
24:05	Serial Number	SXXXNXXXXXXXXX	Serial Number (Vendor Unique, ASCII String), X: Variables
64:25	Model Number	800GB: SAMSUNG MZWLL800HEHP-00003 1.6TB: SAMSUNG MZWLL1T6HEHP-00003 3.2TB: SAMSUNG MZWLL3T2HMJP-00003 6.4TB: SAMSUNG MZWLL6T4HMLS-00003	Model Number (ASCII String)
65:65	PCIe Port 0 Capabilities	03h	Maximum Link Speed (PCIe Gen3)
66:66	PCIe Port 0 Capabilities	04h	Maximum Link Width (x8)
67:67	PCIe Port 1 Capabilities	03h	Maximum Link Speed (PCIe Gen3)
68:68	PCIe Port 1 Capabilities	04h	Maximum Link Width (x8)
69:69	Iniital Power Requirements	07h	12V Power rail initial power requirement (7 W)
71:70	Iniital Power Requirements	0h	Reserved
72:72	Max power Requirement	14h	12V Power rail maximum power requirement (20W)

Bytes	Name	Default Value	Description
74:73	Max power Requirement	0h	Reserved
76:75	Cap List Pointer	0050h	Start Cap Address Pointer (0x50)
79:77	-	0h	-
81:80	-	00A2h	VU Cap ID
83:82	-	0070h	Next Cap Address (0x0070 VU Samsung Specific)
84:84	Sensor Type	02h	-
85:85	Sensor Address	36h	-
87:86	-	0h	Reserved
89:88	Warning Thresh	04E0h	78 Degree Celsius
91:90	OverTemp Thresh	0550h	85 Degree Celsius
92:92	-	FFh	Reserved
93:93	-	FFh	Reserved
94:94	-	FFh	Reserved
95:95	-	FFh	Reserved
96:96	-	FFh	Reserved
97:97	-	FFh	Reserved
98:98	-	FFh	Reserved
99:99	-	FFh	Reserved
100:100	-	FFh	Reserved
101:101	-	FFh	Reserved
102:102	-	FFh	Reserved
103:103	-	FFh	Reserved
104:104	-	FFh	Reserved
105:105	-	FFh	Reserved
106:160	-	FFh	Reserved
107:107	-	FFh	Reserved
108:108	-	FFh	Reserved
109:109	-	FFh	Reserved
110:110	-	FFh	Reserved
111:111	-	FFh	Reserved
113:112	-	00A0h	Dual Port Mode Capability
115:114	-	0074h	Next Cap Address (0x0074 Dual Active/Passive Capability)
117:116	-	00A3h	Dual Active/Passive Capability

Bytes	Name	Default Value	Description
119:118	-	0000h	Next Cap Address (NULL)
120:120	-	03h	Dual Port Vector (Dual Port Passive)
121:121	-	00h	Reserved
122:122	-	00h	Reserved
123:123	-	00h	Reserved
255:124	-	FFh	Reserved

Note: TSE2004av temperature encoding:

Table 7-2: B00 to B15

B15/B07	B14/B06	B13/B05	B12/B04	B11/B03	B10/B02	B09/B01	B08/B00
N/A	N/A	N/A	Sign	128	64	32	16
8	4	2	1	N/A	N/A	N/A	N/A

Note:
The 16-bit value is 2s complement representation of a temperature with the Bit 4 equal to the minimum granularity of 1 °C.
Bit 12 is the sign bit.
For example:

1. a value of 0190h represents 25 °C,
2. a value of 07C0 h represents 124 °C, and
3. a value of 1E80 h represents –24 °C

By choosing the starting of the lowest bit the resolution

8 UEFI EXPANSION ROM

The expansion ROM integrated in Samsung SSD PM1725a supports booting UEFI operating system installed on the drive, it complies to UEFI standard, which is specified in UEFI v2.5 Specification.

8.1 Basic Information

- IA32/x64 architecture support: x64 only
- Binary executable size < 64KB
- Platform BIOS requirement: EFI Specification Revision 2.31+, EFI Shell Version 1.0
- Number of Admin Submission Queue/Admin Completion Queue entries: 2
- Number of IO Queue entries: 2
- Maximum number of IO queues supported: 2
- Interrupt used: None

8.1.1 General Features

- Supports various operating systems booting in UEFI mode
- Ability to boot from large partition (over 2TB) with GUID Partition Table (GPT)
- Provides drive information via UEFI user interface (HII) in pre-boot environment (such as model number, firmware revision and drive capacity)
- Supports Secure Boot
- UEFI standard APIs supporting followings in pre-boot environment (EFI Shell):
  . Basic block read/write access (produced API: EfiBlockIoProtocol)
  . Driver health information (produced API: EfiDriverHealthProtocol)
  . Drive diagnostic function (produced API: EfiDriverDiagnostics2Protocol)
  . NVMHCI functions: GetLogPage, Firmware Download/Activate and Format (produced

API: EfiFirmwareManagementProtocol and NvmExpressPassThruProtocol)

8.2 Supported Operating Systems

Table 8-1: Supported Operating Systems

Index	Operating Systems bootable on the drive
1	Windows Server 2008 R2 64-bit
2	Windows Server 2012 64-bit
3	Windows Server 2012 R2 64-bit
4	Windows Server 2016 64-bit
5	RHEL 6.4 (Kernel 2.6.32)
6	RHEL 6.5 (Kernel 2.6.32)
7	RHEL 6.6 (Kernel 2.6.32)
8	RHEL 7 (Kernel 3.10.0)
9	RHEL 7.1 (Kernel 3.10.0)

Index	Operating Systems bootable on the drive
10	SLES 11 SP3 (Kernel 3.0.13)
11	SLES 12 (Kernel 3.12.28)

9 Product Compliance

Table 9-1: Product Compliance Certifications

Category	Certifications
Safety	c-UL-us
	CE
	TUV
	CB
	CE (EU)
EMC	BSMI (Taiwan)
	KCC (South Korea)
	VCCI (Japan)
	RCM (Australia)
	FCC (USA)

Note
The three existing compliance marks (C-Tick, A-Tick, and RCM) are consolidated into a single compliance mark - the RCM.

10 References

Spec	Reference
PCI Express Base Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress/base3/
NVM Express Specification Rev. 1.2	http://www.nvmexpress.org/
Enterprise SSD Form Factor Version 1.0a	http://www.ssdformfactor.org/
Solid-State Drive Requirements and Endurance Test Method (JESD218A)	http://www.jedec.org/standards-documents/docs/jesd218a
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a